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Quantum Computing for Computer Architects

Second Edition

Tzvetan S. Metodi
Arvin I. Faruque
Frederic T. Chong

***SYNTHESIS LECTURES ON
COMPUTER ARCHITECTURE***

Mark D. Hill, Series Editor

Quantum Computing For Computer Architects Frederic T Chong

Tzvetan S. Metodi, Frederic T. Chong



Quantum Computing For Computer Architects Frederic T Chong:

Quantum Computing for Computer Architects, Second Edition Tzvetan Metodi, Arvin I. Faruque, 2022-06-01

Quantum computers can in theory solve certain problems far faster than a classical computer running any known classical algorithm. While existing technologies for building quantum computers are in their infancy, it is not too early to consider their scalability and reliability in the context of the design of large scale quantum computers. To architect such systems, one must understand what it takes to design and model a balanced fault tolerant quantum computer architecture. The goal of this lecture is to provide architectural abstractions for the design of a quantum computer and to explore the systems level challenges in achieving scalable fault tolerant quantum computation. In this lecture, we provide an engineering oriented introduction to quantum computation with an overview of the theory behind key quantum algorithms. Next, we look at architectural case studies based upon experimental data and future projections for quantum computation implemented using trapped ions. While we focus here on architectures targeted for realization using trapped ions, the techniques for quantum computer architecture design, quantum fault tolerance, and compilation described in this lecture are applicable to many other physical technologies that may be viable candidates for building a large scale quantum computing system. We also discuss general issues involved with programming a quantum computer as well as a discussion of work on quantum architectures based on quantum teleportation. Finally, we consider some of the open issues remaining in the design of quantum computers.

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Quantum Computing for Computer Architects
Tzvetan S. Metodi, Frederic T. Chong, 2022-12-06

Quantum computation may seem to be a topic for science fiction, but small quantum computers have existed for several years, and larger machines are on the drawing table. These efforts have been fueled by a tantalizing property: while conventional computers employ a binary representation that allows computational power to scale linearly with resources, at best, quantum computations employ quantum phenomena that can interact to allow computational power that is exponential in the number of quantum bits in the system. Quantum devices rely on the ability to control and manipulate binary data stored in the phase information of quantum wave functions that describe the electronic states of individual atoms or the polarization states of photons. While existing quantum technologies are in their infancy, we shall see that it is not too early to consider scalability and reliability. In fact, such considerations are a critical link in the development chain of viable device technologies capable of orchestrating reliable control of tens of millions of quantum bits in a large scale system. The goal of this lecture is to provide architectural abstractions common to potential technologies and explore the systems level challenges in achieving scalable fault tolerant quantum computation. The central premise of the

lecture is directed at quantum computation QC architectural issues We stress the fact that the basic tenet of large scale quantum computing is reliability through system balance the need to protect and control the quantum information just long enough for the algorithm to complete execution To architect QC systems one must understand what it takes to design and model a balanced fault tolerant quantum architecture just as the concept of balance drives conventional architectural design For example the register file depth in classical computers is matched to the number of functional units the memory bandwidth to the cache miss rate or the interconnect bandwidth matched to the compute power of each element of a multiprocessor We provide an engineering oriented introduction to quantum computation and provide an architectural case study based upon experimental data and future projection for ion trap technology We apply the concept of balance to the design of a quantum computer creating an architecture model that balances both quantum and classical resources in terms of exploitable parallelism in quantum applications From this framework we also discuss the many open issues remaining in designing systems to perform quantum computation

Quantum Computing for Computer Architects Tzvetan S.

Metodi, Arvin I. Faruque, Frederic T. Chong, 2011 Quantum computation may seem to be a topic for science fiction but small quantum computers have existed for several years and larger machines are on the drawing table These efforts have been fueled by a tantalizing property while conventional computers employ a binary representation that allows computational power to scale linearly with resources at best quantum computations employ quantum phenomena that can interact to allow computational power that is exponential in the number of quantum bits in the system Quantum devices rely on the ability to control and manipulate binary data stored in the phase information of quantum wave functions that describe the electronic states of individual atoms or the polarization states of photons While existing quantum technologies are in their infancy we shall see that it is not too early to consider scalability and reliability In fact such considerations are a critical link in the development chain of viable device technologies capable of orchestrating reliable control of tens of millions quantum bits in a large scale system The goal of this lecture is to provide architectural abstractions common to potential technologies and explore the systems level challenges in achieving scalable fault tolerant quantum computation

Deep Learning for Computer Architects Brandon Reagen, Robert Adolf, Paul Whatmough, Gu-Yeon Wei, David Brooks, 2022-05-31 Machine learning and specifically deep learning has been hugely disruptive in many fields of computer science The success of deep learning techniques in solving notoriously difficult classification and regression problems has resulted in their rapid adoption in solving real world problems The emergence of deep learning is widely attributed to a virtuous cycle whereby fundamental advancements in training deeper models were enabled by the availability of massive datasets and high performance computer hardware This text serves as a primer for computer architects in a new and rapidly evolving field We review how machine learning has evolved since its inception in the 1960s and track the key developments leading up to the emergence of the powerful deep learning techniques that emerged in the last decade Next we review representative workloads including

the most commonly used datasets and seminal networks across a variety of domains In addition to discussing the workloadsthemselves we also detail the most popular deep learning tools and show how aspiring practitioners can use the tools with the workloads to characterize and optimize DNNs The remainder of the book is dedicated to the design and optimization of hardware and architectures for machine learning As high performance hardware was so instrumental in the success of machine learning becoming a practical solution this chapter recounts a variety of optimizations proposed recently to further improve future designs Finally we present a review of recent research published in the area as well as a taxonomy to help readers understand how various contributions fall in context

Quantum Computer Systems Yongshan Ding,2020-06-17 This book targets computer scientists and engineers who are familiar with concepts in classical computer systems but are curious to learn the general architecture of quantum computing systems It gives a concise presentation of this new paradigm of computing from a computer systems point of view without assuming any background in quantum mechanics As such it is divided into two parts The first part of the book provides a gentle overview on the fundamental principles of the quantum theory and their implications for computing The second part is devoted to state of the art research in designing practical quantum programs building a scalable software systems stack and controlling quantum hardware components Most chapters end with a summary and an outlook for future directions This book celebrates the remarkable progress that scientists across disciplines have made in the past decades and reveals what roles computer scientists and engineers can play to enable practical scale quantum computing

Computer Architecture Techniques for Power-Efficiency Stefanos Kaxiras,Margaret Martonosi,2022-06-01 In the last few years power dissipation has become an important design constraint on par with performance in the design of new computer systems Whereas in the past the primary job of the computer architect was to translate improvements in operating frequency and transistor count into performance now power efficiency must be taken into account at every step of the design process While for some time architects have been successful in delivering 40% to 50% annual improvement in processor performance costs that were previously brushed aside eventually caught up The most critical of these costs is the inexorable increase in power dissipation and power density in processors Power dissipation issues have catalyzed new topic areas in computer architecture resulting in a substantial body of work on more power efficient architectures Power dissipation coupled with diminishing performance gains was also the main cause for the switch from single core to multi core architectures and a slowdown in frequency increase This book aims to document some of the most important architectural techniques that were invented proposed and applied to reduce both dynamic power and static power dissipation in processors and memory hierarchies A significant number of techniques have been proposed for a wide range of situations and this book synthesizes those techniques by focusing on their common characteristics

Table of Contents Introduction Modeling Simulation and Measurement Using Voltage and Frequency Adjustments to Manage Dynamic Power Optimizing Capacitance and Switching Activity to Reduce Dynamic Power Managing Static Leakage Power

Conclusions **On-Chip Networks** Natalie Enright Jerger, Tushar Krishna, Li-Shiuan Peh, 2017-06-19 This book targets engineers and researchers familiar with basic computer architecture concepts who are interested in learning about on chip networks This work is designed to be a short synthesis of the most critical concepts in on chip network design It is a resource for both understanding on chip network basics and for providing an overview of state of the art research in on chip networks We believe that an overview that teaches both fundamental concepts and highlights state of the art designs will be of great value to both graduate students and industry engineers While not an exhaustive text we hope to illuminate fundamental concepts for the reader as well as identify trends and gaps in on chip network research With the rapid advances in this field we felt it was timely to update and review the state of the art in this second edition We introduce two new chapters at the end of the book We have updated the latest research of the past years throughout the book and also expanded our coverage of fundamental concepts to include several research ideas that have now made their way into products and in our opinion should be textbook concepts that all on chip network practitioners should know For example these fundamental concepts include message passing multicast routing and bubble flow control schemes Multi-Core Cache Hierarchies Rajeev Balasubramanian, Norman Paul Jouppi, Naveen Muralimanohar, 2011 A key determinant of overall system performance and power dissipation is the cache hierarchy since access to off chip memory consumes many more cycles and energy than on chip accesses In addition multi core processors are expected to place ever higher bandwidth demands on the memory system All these issues make it important to avoid off chip memory access by improving the efficiency of the on chip cache Future multi core processors will have many large cache banks connected by a network and shared by many cores Hence many important problems must be solved cache resources must be allocated across many cores data must be placed in cache banks that are near the accessing core and the most important data must be identified for retention Finally difficulties in scaling existing technologies require adapting to and exploiting new technology constraints The book attempts a synthesis of recent cache research that has focused on innovations for multi core processors It is an excellent starting point for early stage graduate students researchers and practitioners who wish to understand the landscape of recent cache research The book is suitable as a reference for advanced computer architecture classes as well as for experienced researchers and VLSI engineers Table of Contents Basic Elements of Large Cache Design Organizing Data in CMP Last Level Caches Policies Impacting Cache Hit Rates Interconnection Networks within Large Caches Technology Concluding Remarks A Primer on Memory Consistency and Cache Coherence Daniel Sorin, Mark Hill, David Wood, 2022-11-10 Many modern computer systems and most multicore chips support shared memory in hardware In a shared memory system each of the processor cores may read and write to a single shared address space For a shared memory machine the memory consistency model defines the architecturally visible behavior of its memory system Consistency definitions provide rules about loads and stores or memory reads and writes and how they act upon memory As part of supporting a memory consistency model many

machines also provide cache coherence protocols that ensure that multiple cached copies of data are kept up to date The goal of this primer is to provide readers with a basic understanding of consistency and coherence This understanding includes both the issues that must be solved as well as a variety of solutions We present both highlevel concepts as well as specific concrete examples from real world systems Table of Contents Preface Introduction to Consistency and Coherence Coherence Basics Memory Consistency Motivation and Sequential Consistency Total Store Order and the x86 Memory Model Relaxed Memory Consistency Coherence Protocols Snooping Coherence Protocols Directory Coherence Protocols Advanced Topics in Coherence Author Biographies *A Primer on Memory Consistency and Cache Coherence, Second Edition* Vijay Nagarajan, Daniel J. Sorin, Mark D. Hill, David A. Wood, 2022-05-31 Many modern computer systems including homogeneous and heterogeneous architectures support shared memory in hardware In a shared memory system each of the processor cores may read and write to a single shared address space For a shared memory machine the memory consistency model defines the architecturally visible behavior of its memory system Consistency definitions provide rules about loads and stores or memory reads and writes and how they act upon memory As part of supporting a memory consistency model many machines also provide cache coherence protocols that ensure that multiple cached copies of data are kept up to date The goal of this primer is to provide readers with a basic understanding of consistency and coherence This understanding includes both the issues that must be solved as well as a variety of solutions We present both high level concepts as well as specific concrete examples from real world systems This second edition reflects a decade of advancements since the first edition and includes among other more modest changes two new chapters one on consistency and coherence for non CPU accelerators with a focus on GPUs and one that points to formal work and tools on consistency and coherence

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